Application Note

NOVOSENSE

Common Questions for Isolated Amplifier NSI1311

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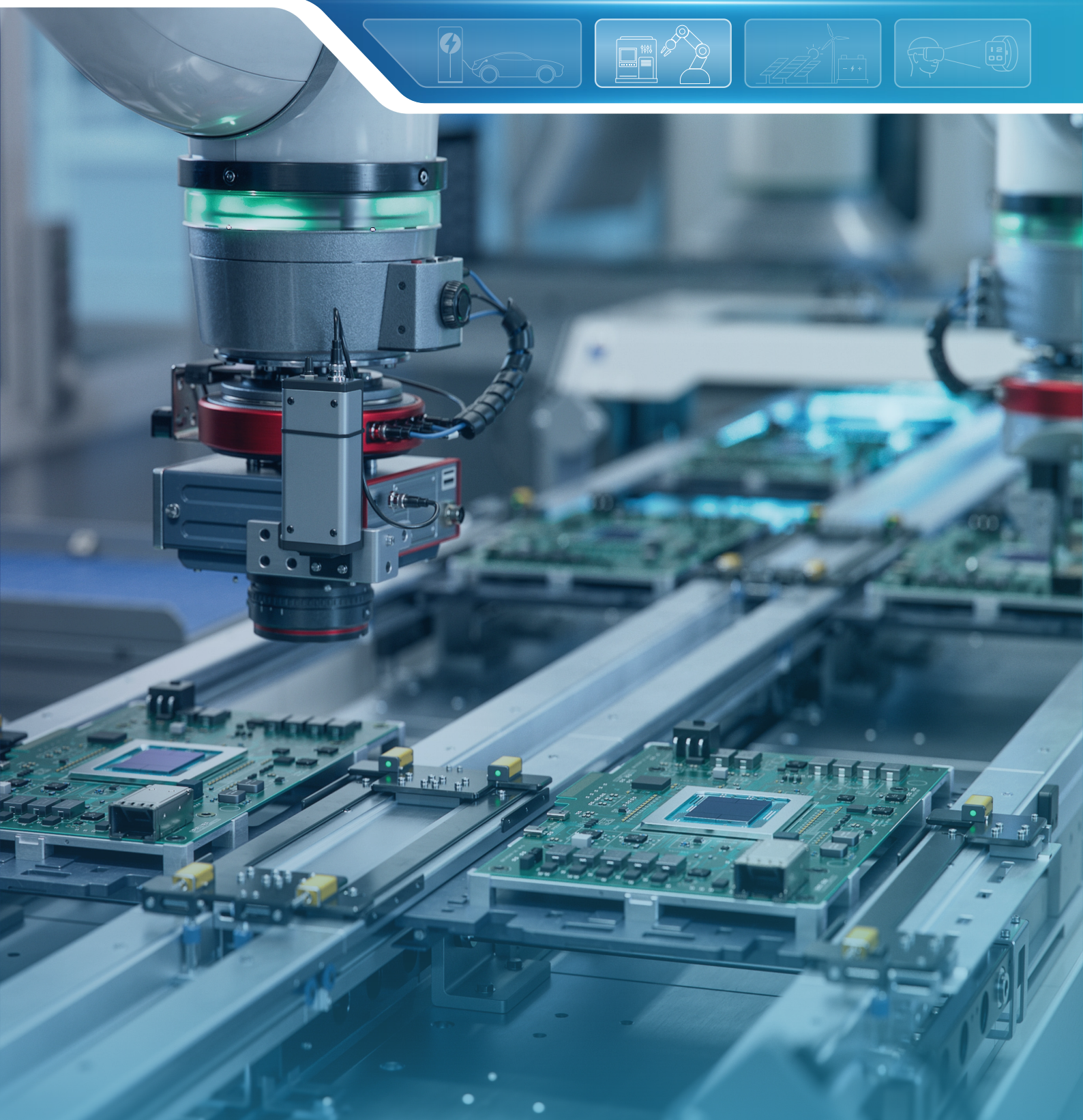
Author: Jiahua Xu, Michelle Zhao



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ABSTRACT

In high-voltage industrial applications, isolated sensing protects low-voltage circuits from dangerous high-voltage power circuits while ensuring communication between different voltage domains, which significantly improves system reliability.

The Novosense NSI12xx/NSI13xx series isolated sensing products have been widely used in industrial control, industrial power supply, electric vehicles and other applications. The NSI1311 is a high-performance isolated amplifier with a high input impedance that accept wide range single-ended input. The single-ended input is suited to bus voltage monitoring in high voltage applications where isolation is required. To simplify the customer's design, the Q&A introduces how to apply NSI1311 according to the customer's demand of voltage sensing.

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1.Typical Application Circuit

The NSI1311 has an input impedance of up to 1GΩ and has a wide input voltage range of 0.02~2V. These features make the NSI1311 ideally suitable for isolated DC voltage sensing applications such as frequency inverters and servo drives. The typical application circuit is shown in Figure 1.

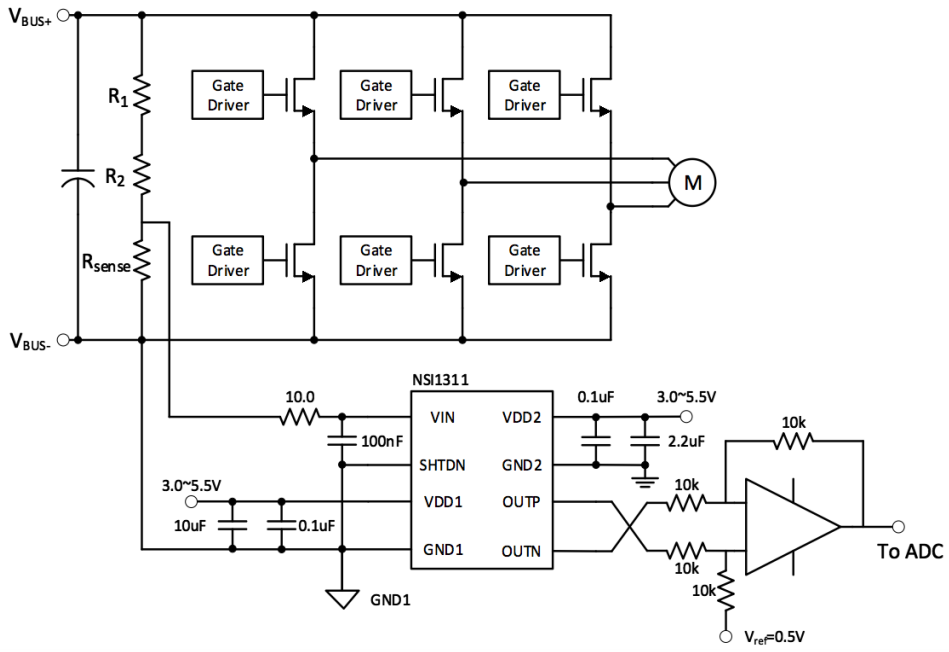

Figure 1. Typical application circuit in voltage sensing

2.Q&A for Voltage Sensing Application

2.1.How to design input conditioning circuit

The high voltage in customer's system is divided by a resistance network, and the divided voltage is applied to the input of the NSI1311 through a RC filter to ensure best performance. The RC filter is shown as RFLT and CFLT in Figure 2. The characteristics of this filter are dictated by the input topology and sensing frequency of the ADC, customers can adjust the filter design by demand.

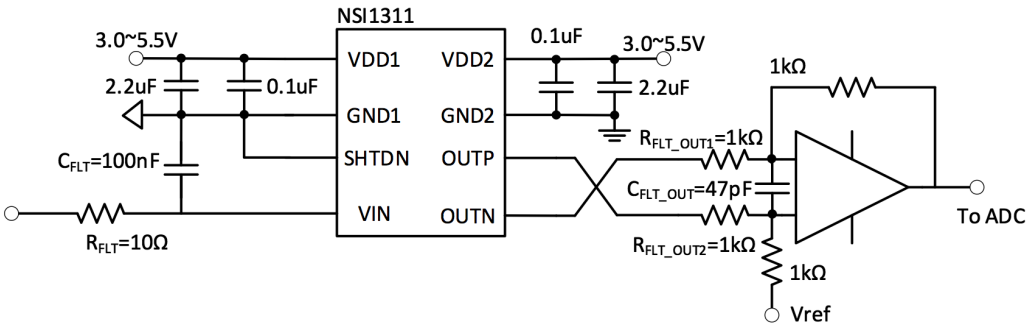

Figure 2. Typical single-ended to differential output circuit for NSI1311

The cut-off frequency of the RC filter is as below:

$$f_C = \frac{1}{2\pi R_{FLT} C_{FLT}}$$

2.2.How to understand differential output conversion

The differential output of the isolated amplifier with common-mode voltage of 1.4V (typ) can be converted to a single-ended analog output. Differential output is highly recommended in common mode immunity application. The differential output of NSI1311 can be expressed as:

$$V_{OUTP} - V_{OUTN} = Gain * V_{IN}$$

$$V_{OUTP} = V_{CMout} + \frac{1}{2} * Gain * V_{IN}$$

$$V_{OUTN} = V_{CMout} - \frac{1}{2} * Gain * V_{IN}$$

where VIN is the input voltage, V_{OUTP} and V_{OUTN} are respectively the positive and negative output voltage. With the common-mode voltage V_{CMout} of 1.4V (typ), the OUTN and OUTP pins can not be connected to ground directly. If the OUTN or OUTP pins are shorted to the VDD2 pin or the GND2 pin, the short-circuit current will be limited to around 14mA by the internal output circuit of NSI1311.

The typical differential to single-ended output circuit is shown in Figure 2. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current. The recommended load capacitance that is directly connected between OUTP and OUTN is less than 330pF. Excessive load capacitance may cause waveform distortion of NSI1311 output when sensing dynamic signals. The cut-off frequency of the differential output filter can be calculated as:

$$f_{C\_OUT} = \frac{1}{2\pi(R_{FLT\_OUT1} + R_{FLT\_OUT2}) * C_{FLT\_OUT}}$$

2.3.How to select filter capacitor at the power supply pin

For the applications with noisy working conditions (such as motor control), or power supply circuits that need improvement (such as long wiring of the front power supply), special attention should be paid to the design of the NSI1311 power supply pin. Optocoupler isolation products require a 0.1uF capacitor placed nearby the power supply pin. While for the NSI1311, it is recommended that depending on the supply voltage waveform of the customer's system, a voltage stabilizing capacitor of more than 2.2uF should be connected in parallel with the 0.1uF bypass capacitor placed nearby to achieve better filtering effect. Customers can also increase the value of the original capacitor from 0.1uF to more than 2.2uF to improve the filtering effect without PCB revision.

2.4.What is fail-safe function (missing VDD1 detection)

The NSI1311 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The failsafe waveform is shown in Figure 3. The typical failsafe output is -2.53V (typ) when VDD1 undervoltage.
The fail-safe output does not occur under normal device operation, and it will only be activated in following conditions:

- When the undervoltage of VDD1 is detected (VDD1< VDD1UV).
- When SHTDN signal is activated (pulled high).

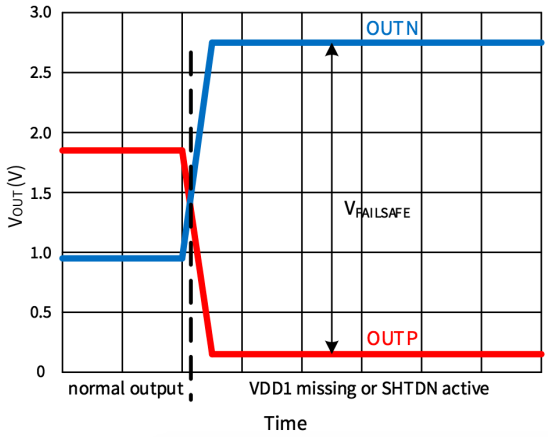

Figure 3. Typical failsafe output when VDD1 undervoltage for NSI1311

Attention should be paid to the power-up and power-down sequence to prevent the NSI1311 from entering fail-safe mode when VDD1 has no power and VDD2 is on, which will cause system alarm. During power-down, the filter capacitor of VDD1 can be increased so that VDD1 changes more slowly than VDD2 to solve this problem.

2.5.How to calculate sensing error

The error of voltage sensing mainly consists of the resistance error of the voltage dividing resistance network, the error of the sensing IC, the error of the post-conditioning circuit and the error of MCU signal processing. When the sensing accuracy is abnormal, it is necessary to check the output of the sensing signal chain step by step to locate which stage of the circuit introduces the error. The calculation of sensing error introduced by the NSI1311 is discussed in this section.

The sensing error introduced by the sensing IC NSI1311 consists of input offset voltage Vos, Gain error EG, Nonlinearity and their temperature drift. With high frequency ripple on the supply voltage, the output accuracy may be influenced because of the limited AC power supply rejection ratio PSRRac. If it unfortunately occurs, the customers should add the decoupling capacitance of the power supply and optimize PCB layout refer to Section 3.

The error introduced by Vos can be calculated as:

$$Error\_Vos = \sqrt{(\frac{Vos_{max} + TC_{vos} * Tv}{Vin} \times 100\%)^2}$$

Vos_{max} is the maximum value of input offset voltage at 25°C, ±1.5mV for NSI1311 as specified in the specification. TC_{vos} is the maximum input offset drift. Tv is the range of the temperature variation. Vin is the input voltage in customers' applications.

The error introduced by EG can be calculated as:

$$Error\_EG = \sqrt{(EGmax + TC_{EG} * Tv)^2}$$

EG_{max} and TC_{EG} are respectively the maximum gain error at 25°C and its maximum thermal drift, ±0.3% and ±45ppm/°C for NSI1311 as specified in the specification.

The error introduced by Nonlinearity is $Nonlinearity_{max}$, the maximum value of Nonlinearity in the entire temperature range -40°C to 125°C, ±0.04% during VIN=0.1V~2V for NSI1311 as specified in the specification.

The maximum sensing error introduced by NSI1311 is expressed as:

$$Error\_NSI1311 = \sqrt{Error\_Vos^2 + Error\_EG^2 + Nonlinearity_{max}{}^2}$$

For example, consider a NSI1311 with the sensing input voltage of 2V and a - 40°C to 85°C temperature range. The total error calculation is shown in Table 1.

Table 1. Total Error Calculation of NSI1311 (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=2V	Error at Vin=0.1V
Input offset error	Error_Vos	$Error_{Vos} = \sqrt{(\frac{Vos_{max} + TC_{vos} * Tv}{Vin} \times 100\%)^2} = \sqrt{(\frac{\pm 1.5\text{mV} + 30\mu\text{V/°C} * 60\text{°C}}{Vin} \times 100\%)^2}$	±0.165%	±3.3%
Gain error	Error_EG	$Error\_EG = \sqrt{(EGmax + TC_{EG} * Tv)^2} = \sqrt{(\pm 0.3\% + \pm 45\text{ppm/°C} * 65\text{°C})^2}$	±0.593%	±0.593%
Nonlinearity	$Nonlinearity_{max}$	$Nonlinearity_{max} = \pm 0.04\%$	±0.04%	±0.04%
Total error	Error_NSI1311	$Error\_NSI1311 = \sqrt{Error\_Vos^2 + Error\_EG^2 + Nonlinearity_{max}{}^2}$	±0.616%	±3.353%

The total error is strongly related to the input voltage Vin, especially when VIN is at a low level. In the table above, the total error is 0.616% at Vin=2V and 3.353% at Vin=0.1V. If the input voltage is a small value, Error_Vos accounts for a large ratio because Vin is in the denominator. If Vin is the full range, the total error is approximately the combination of Gain error and Nonlinearity. The thermal drift error is negligible when the NSI1311 operate at room temperature.
For higher accuracy, the input offset voltage and Gain error at 25°C can be corrected through software calibration. Take the error calculation in table 1 as an example. The total error at Vin=2V can be reduced from ±0.616% to ±0.309% with software calibration. The calculation process is shown in Table 2.

Table 2. Total Error Calculation of NSI1311 with Software Calibration (- 40°C to 85°C)

Error Component	Symbol	Equation	Error at Vin=2V	Error at Vin=0.1V
Input offset error	Error_Vos	$Error_{Vos} = \sqrt{(\frac{TC_{vos} * Tv}{Vin} \times 100\%)^2}$ $= \sqrt{(\frac{30\mu V/°C * 60°C}{Vin} \times 100\%)^2}$	±0.09%	±1.8%
Gain error	Error_EG	$Error\_EG = \sqrt{(TC_{EG} * Tv)^2} = \sqrt{(\pm 45ppm/°C * 65°C)^2}$	±0.293%	±0.293%
Nonlinearity	Nonlinearitymax	$Nonlinearity_{max} = \pm 0.04\%$	±0.04%	±0.04%
Total error	Error_NSI1311	$Error\_NSI1311 = \sqrt{Error\_Vos^2 + Error\_EG^2 + Nonlinearity_{max}{}^2}$	±0.309%	±1.824%

3.Q&A for PCB Layout

3.1.Basic PCB layout consideration

The layout example for the NSI1311 is shown in Figure 4. There are some key guidelines or considerations for optimizing performance in PCB layout:

- The NSI1311 requires a 0.1μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used. The external power supply is connected through the pads of the bypass capacitors and then to the chip for better decoupling and filtering.
- The space under the chip should keep free from planes, traces, pads and via for good insulation performance. Additionally, the trace under the chip may couple the dipole radiation energy of the isolator and act as an antenna, affecting EMI performance.
- Place the sense resistor close to the VIN pin. Kelvin rules is recommended for the connection between the sense resistor to the NSI1311. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.

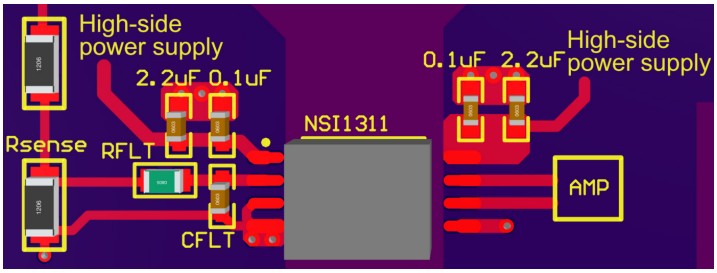

Figure 4. Layout example for NSI1311

3.2.How do we optimize EMI performance through PCB layout

In system design, some applications need to pass emission tests, such as CISPR25 standard for automotive applications and CISPR32 for industrial applications. For isolation products like NSI1311, the radiation mainly comes from the dipole emissions of the isolation barrier. Some PCB design considerations are listed as follows for EMI optimization:

- For low-frequency conductive noise under 10MHz, add the appropriate EMI filter is a good manner.
- To suppress radiation on the power lines, place Ferrite Beads respectively in series with the line of VDD and GND for filter as is shown in Figure 5. The ferrite Beads, together with decoupling capacitors, can filter and isolate noise well. In the layout area, the ferrite beads need to effectively separate the chip layout area from peripheral circuit without overlap in different PCB layers.
- Add a safety stitching Y capacitor (shown in Figure 5) between GND1 and GND2 as close as possible to provide a return path for common-mode noise through the isolation barrier. Larger capacitance means smaller high-frequency impedance and is better for current returning. The leakage current and withstand voltage should also be considered when selecting a safety rated capacitor. In PCB design, pay attention to minimizing the parasitic inductance and parasitic impedance of the capacitor connection line.

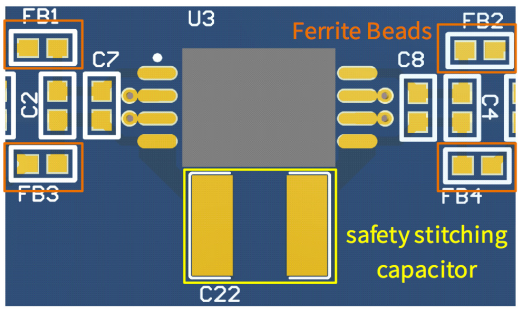

Figure 5. Layout example for EMI optimization

Another thing to consider is Edge emissions of PCB, which occurs at the edges of ground and power planes. The following points should be noted to reduce Edge emissions of PCB.

- Do not route high-frequency signal lines near the edge of the PCB.
- Align the outer edges of the ground and power planes.
- Add a ground guard ring structure laced together by vias around the PCB.

4.Revision History

Revision	Description	Author	Date
1.0	Initial version	Jiahua Xu, Michelle Zhao	24/5/2024

Sales Contact: sales@novosns.com;Further Information: www.novosns.com